UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/821,713	04/09/2004	Hideki Sawada	10921.215US01	1532

7590 09/04/2008

HAMRE, SCHUMANN, MULLER & LARSON, P.C.
P. O. BOX 2902-0902
MINNEAPOLIS, MN 55402

EXAMINER	
LE, TUAN H	

ART UNIT	PAPER NUMBER
2622	

MAIL DATE	DELIVERY MODE
09/04/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/821,713	SAWADA, HIDEKI	
	Examiner	Art Unit	
	TUAN H. LE	2622	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 May 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4 and 6-9* is/are rejected.

7)☒ Claim(s) *5* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

Applicant's arguments filed 5/20/08 have been fully considered but they are not persuasive.

Regarding **claims 1 and 8**, the applicant submits that Kozuka (US 6,473,538) does not disclose "a reset signal being generated based on both the resolution data and clock signal", Remarks, pg. 5 lines 21-24. However, the examiner respectfully disagrees.

On the other hand, Kozuka discloses "a reset signal being generated based on both the resolution data and clock signal", (Kozuka, Fig. 5, Fig. 6, and Fig. 8, wherein reset signals for M4a is inherent part of timing generator 5 and switching means 10).

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-2 and 6-9 are rejected under 35 U.S.C. 102(e) as being anticipated by Kozuka (U.S. Pat. 6,473,538).

Regarding **claim 1**, Kozuka discloses an image reading apparatus (Kazuka, column 3 lines 60-67, wherein an image reading apparatus using an image sensor with plurality of photoelectric conversion devices) comprising:

a plurality of image sensor chips (shift register 3 and light-receiving element arrays 4) each of which includes a plurality of photoelectric conversion elements (PDa) and performs outputting (by M1a) of electric charge accumulated due to light received by the photoelectric conversion elements and resetting (M4a) of the accumulated electric charge (Kozuka, Fig. 5, Fig. 6, Fig. 8, column 6 lines 19-23 and lines 32-37, wherein an image sensor includes many photoelectric conversion devices with photodiode arrays); and

a plurality of control chips (timing generator 5 and switching means 10) for controlling operation of the image sensor chips, (Kozuka, Fig. 8, switching means 10 inputs resolution data);

wherein each of the control chips (timing generator 5 and switching means 10) includes a resolution data input section (mode 1 and mode 2) to which resolution data to specify resolution is inputted (Kozuka, column 9 lines 17-24, wherein high resolution, intermediate resolution, and low resolution are available), a clock signal input section for input of a clock signal (Kozuka, Fig. 8 wherein 5 receives clock signal), and also includes a reset signal generator (inherent part) for generating a reset signal for performing the resetting of the electric charge in a cycle corresponding to the resolution data inputted into the resolution data input section (Kozuka, Fig. 5 and Fig.8, wherein reset signals for M4a is inherent part of timing generator 5 and switching means 10),

the reset signal being generated based on both the resolution data and the clock signal (Kozuka, Fig. 5, Fig. 6, and Fig. 8, wherein reset signals for M4a is inherent part of timing generator 5 and switching means 10).

Regarding **claim 2**, Kozuka discloses all of the limitations of claim 1. In addition, Kozuka discloses each of the control chips (timing generator 5 and switching means 10) comprises a resolution void terminal (mode 1 and mode 2) for selectively inhibiting image reading at a predetermined resolution (Kozuka, Fig. 8), the image reading at the predetermined resolution being inhibited when the resolution void terminal is held in a first wiring state (at least one of two bits is high) but being enabled when the resolution void terminal is held in a second wiring state different from the first wiring state (both two bits are low), (Kozuka, Fig. 8, wherein as for mode 1 and mode 2, 00 represents void terminal, 01 represents high resolution, 10 represents intermediate resolution, 11 represents low resolution).

Regarding **claim 6**, Kozuka discloses all of the limitations of claim 1. In addition, Kozuka discloses each of the image sensor chips (shift register 3 and light-receiving element arrays 4) is a CCD image sensor chip including photodiodes (PDa), a line memory (14) and an analog shift register (11), (Kozuka, Fig. 6, wherein structure of image chip is shown); and

wherein each of the control chips (time generator 5 and switching means 10) generates signals for causing the photodiodes to transmit electric charge to the line memory and the analog shift register and signals for causing the analog shift register to output signals, the signals outputted from the analog shift register being inputted into

the control chip (Kozuka, Fig. 8 and column 2 lines 40-47, wherein time generator 5 drives light-receiving arrays 4 and shift registers 3).

Regarding **claim 7**, Kozuka discloses all of the limitations of claim 1. In addition, Kozuka discloses the control chips (time generator 5 and switching means 10) include amplifiers (amplifiers 6) for amplifying signals outputted from the image sensor chips, and

wherein a reference voltage is applied to the amplifiers in parallel from a common power supplier (Kozuka, Fig. 8 and column 2 lines 55-60, wherein signal output amplifiers 6 and 6' are available).

Regarding **claim 8**, Kozuka discloses a control chip (timing generator 5 and switching means 10) for controlling driving of an image sensor chip (light-receiving elements 4), the control chip comprising:

a clock signal input section for input of a clock signal (Kozuka, Fig. 8 wherein 5 receives clock signal);

a resolution data input section (mode 1 and mode 2) to which resolution data to specify resolution is inputted (Kozuka, column 9 lines 17-24, wherein high resolution, intermediate resolution, and low resolution are available); and

a reset signal generator (inherent part) for generating a reset signal for causing the image sensor chip to reset accumulated electric charge in a cycle corresponding to the resolution data inputted into the resolution data input section (Kozuka, Fig. 5 and Fig.8, wherein reset signals for M4a is inherent part of timing generator 5 and switching means 10), the reset signal being generated based on both the resolution data and the

clock signal (Kozuka, Fig. 5, Fig. 6, and Fig. 8, wherein reset signals for M4a is inherent part of timing generator 5 and switching means 10).

Regarding **claim 9**, Kozuka discloses all of the limitations of claim 8. In addition, Kozuka discloses a resolution void terminal (Kozuka, Fig. 8, mode 1 and mode 2), wherein image reading at a predetermined resolution is inhibited when the resolution void terminal is held in a predetermined wiring state (Kozuka, Fig. 8, wherein as for mode 1 and mode 2, 00 represents void terminal, 01 represents high resolution, 10 represents intermediate resolution, 11 represents low resolution).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 3-4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kozuka (U.S. Pat. 6,473,538) and further in view of Lowen (U.S. Pat. 5,373,372).

Regarding **claim 3**, Kozuka discloses all of the limitations of claim 1. Furthermore, Kozuka discloses the resolution data input section comprises a first input terminal and a second input terminal (Kozuka, Fig. 8 and column 8 lines 46-52, wherein two terminals mode 1 and mode 2 are used for resolution data input) and wherein each of control chips (timing generator 5 and switching means 10), is set to a first mode , the first mode permitting parallel input of the resolution data into the first input terminal and second input terminal (Kozuka, Fig. 8, wherein mode1 and mode1 are two terminals).

However, Kozuka does not disclose a second mode, the second mode permitting serial input of the resolution data into the second input terminal.

On the other hand, Loewen discloses a second mode (resolution selection inputs on a serial interface), the second mode permitting serial input of the resolution data into the second input terminal (Loewen, Fig. 1 and column 4 lines 25-32, wherein resolution selection means 24 is used for serial resolution data input).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to implement the resolution means as described by Loewen into the image reading apparatus as described by Kozuka for receiving resolution data input in serial mechanism because such implementation is capable of scanning at multiple resolutions which does not require significant processing capability, does not require a complex paper advance or scanner advance mechanism, and which is inexpensive and relatively simple to implement (Loewen, column 2 lines 16-21).

Regarding **claim 4**, Kozuka and Loewen disclose all of the limitations of claim 3. In addition, Loewen discloses a mode setting terminal (resolution selection means 24) for selection of the first mode (parallel interface) and the second mode (serial interface), and wherein only one of the first mode and the second mode is selected when the mode setting terminal is grounded (Loewen, Fig. 1 and column 4 lines 25-32, wherein resolution selection means 24 is used for parallel/ serial resolution data input).

Allowable Subject Matter

Claim 5 is objected to as being dependent upon a rejected base claim 3, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

More specifically, the prior art of record neither anticipates nor renders obvious the limitation of "image reading at a predetermined resolution is inhibited when the second mode is selected and the first input terminal is held in a predetermined wiring state.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Kozuka (U.S. 6,531,690).

Mandai et al (U.S. Pat. 5,744,379).

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tuan H. Le whose telephone number is (571) 270-1130. The examiner can normally be reached on M-Th 7:30-5:00 F 7:30-4:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David L. Ometz can be reached on (571) 272-7593. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/David L. Ometz/
Supervisory Patent Examiner, Art Unit 2622

/Tuan Le/